ULTRA LOW PHASE NOISE 1 GHz OCXO

R. Boroditsky, J. Gomez,
NEL Frequency Controls, 357 Beloit Street, Burlington, WI 53105

Abstract

Modern radar equipment, commercial and defense communication systems, point-to-point and point-to-multipoint microwave digital radios, microwave sources require excellent stability, extremely low phase noise frequency sources in UHF band. Existing HF OCXO at 100 MHz can achieve –90 dBc/Hz phase noise at 10 Hz offset from the carrier and -125dBc/Hz at 100 Hz offset. The goal of this work was to create a 1 GHz OCXO with temperature stability performance of SC-cut (1E-8 or better), with the similar to 100 MHz phase noise close to the carrier, and noise floor reaching -150 dBc/Hz, while providing +7 dBm of output power. The goal was accomplished by integrating in a small SMD package (20x25mm), or Europack (36x25 mm) high performance, low frequency, SC-cut reference OCXO, low noise off-the-shelf Phase Lock Loop (PLL) IC, and ultra low noise 1 GHz VCXO. Reference OCXO implemented in DIP14 compatible format was described in previous papers. The key solutions for this development were optimization of the phase noise performance both close to the carrier frequency and on the noise floor, and design of a VCXO. The VCXO is based on a 3rd overtone 200 MHz AT-cut crystal resonator with relatively high Q, passive band-pass filter, tuned on the fifth harmonic of the 200 MHz VCXO, and a free-running L-C oscillator, which is injection locked to the above mentioned fifth harmonic of the VCXO. Dual stage multiplication of the lower frequency VCXO (100.00 MHz, and 111.111 MHz), and additional measures of phase noise reduction far away from the carrier were also investigated.

Introduction

High stability, low phase noise frequency source is an essential part of modern radar equipment, microwave radios, telecommunication equipment, etc. Some applications require low frequency SC-cut temperature stability (low ppb) and aging (<1 ppb/day), at the same time with close-in phase noise close to -90 dBc/Hz at 10 Hz offset from the carrier, and the noise floor reaching -150 dBc/Hz at carrier frequency of 1 GHz. Above mentioned parameters in combination with small size and low power consumption present design challenges, which are addressed in this paper.

Design concept

The block diagram of the device is shown on Fig.1.

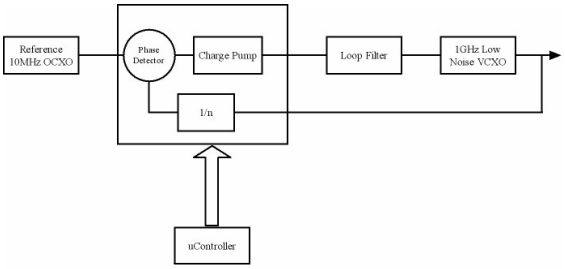

Fig. 1. Block Diagram.

The reference OCXO is realized in DIP14 compatible package using described in previous papers internally heated resonator technology. Temperature stability of the reference is about ± 10 ppb over -30 to 70 ºC range. Steady state power consumption at room temperature is 100 mW. Phase noise (smoothed curve) is shown in Fig. 2.

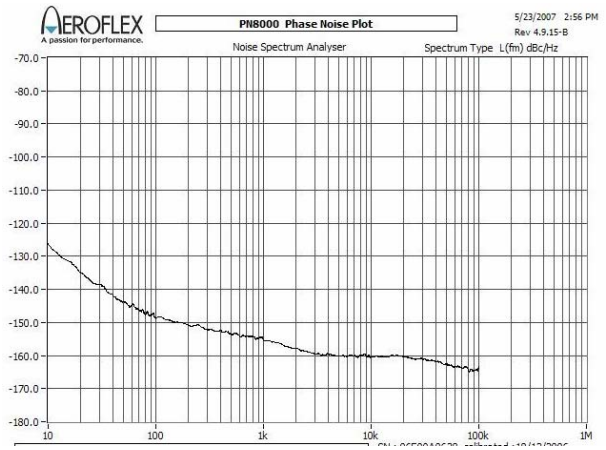

Fig.2. Reference OCXO phase noise.

The PLL circuit incorporated commercial "off-the-shelf" PLL IC, and a loop filter. It is controlled by microcontroller, which sets internal to the IC divider coefficients, as well as provides reliable start-up operation during power-on, power-off transitions. Loop filter bandwidth is determined by the phase noise requirements and the quality of the reference oscillator. With high performance OCXO based on overtone SC-cut being used as a reference, the optimal loop bandwidth would be set at the frequency where VCXO phase noise plot intersects the one of the OCXO + 20logN, where N is the ratio of the VCXO frequency and the reference. This in our case would be 500 – 700 Hz. The problem here is the phase noise produced by the PLL itself. The optimum bandwidth had to be narrowed to about 100 Hz and settle for the phase noise outside of it of that of the VCXO. Selection of the comparison frequency is based on the spectrum purity of the output signal requirement, as well as limitations of the physical size of the components of the loop filter. Influence of the PLL noise also had to be taken into account. Optimization of the latter led to requirement of the comparison frequency to be as high as possible. In order to implement that the frequency of the reference OCXO was multiplied by 5 to be able to compare at 50 MHz. Design provides flexibility of taking the feedback signal either from the UHF VCXO output or from the oscillator output before multiplication. The latter case allows the use of lower frequency, less expensive PLL IC. The physical design of the device is modular. The motherboard, which has 22x25 mm^2 dimensions, contains PLL circuit, loop filter, microcontroller, and output amplifier with matching network. VCXO is built as a separate module.

1 GHz VCXO design

Original concept of VCXO design was similar to the one described in [1]. Simplified VCXO circuit with corresponding spectrum of each stage is shown on Fig.6. Since the reference oscillator provides frequency stability over all conditions of less than ± 0.5 ppm, worst case, the absolute pull range (APR) of the VCXO can be just a few ppm wider than that value. It allows the use of 3^{rd} overtone crystal, which leads to improved phase noise performance, especially at frequency offsets closer to the carrier. The sustaining stage is realized as a CMOS gate Pierce oscillator with relatively high crystal drive level to attain low phase noise level on the noise floor. Since, as mentioned above, the overall stability of the VCXO requirement is rather loose it does not present a major problem. The choice of VCXO frequency to be multiplied up to 1 GHz presented some challenges as well. The natural choice is 200 MHz. The advantages include simplicity of multiplication – just selection of 5^{th} harmonic – and lower multiplication factor. The drawbacks, however, - higher cost of crystal resonator, and higher phase noise both close to the carrier and on the noise floor did not make this a better choice. Another frequency of interest was $1/9^{th}$ of 1 GHz – i.e. 111.111 MHz. It can be multiplied in 2 stages (x3 and x3), has very good noise floor, but in this case comparison frequency would have to be low – around 100 KHz with available divider coefficients of the PLL. That would

create problems with phase noise in the frequency offsets from 10 Hz to several KHz. So, the choice falls into 100 MHz frequency for VCXO. The multiplication is also realized in 2 stages (x5 and x2), which is not as convenient as in case of 111.111 MHz, but comparison frequency could be set at 50 MHz, which improves phase noise performance in the midsection frequency offsets from the carrier due to PLL IC limitations. The phase noise of 100 MHz VCXO is shown in Fig.3.

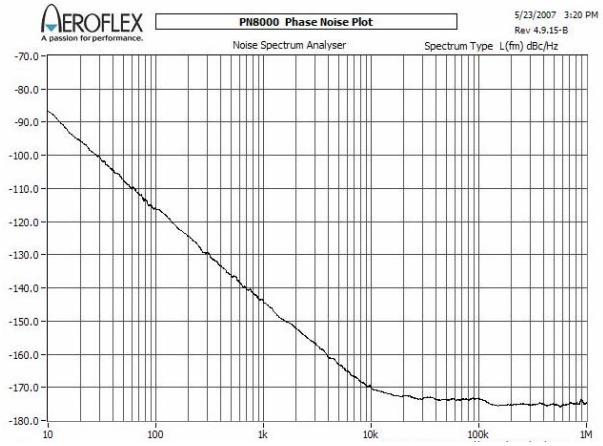

Fig. 3. 100 MHz VCXO Phase Noise

Two stage multiplier was realized using CMOS gates and Chebyshev filters. The biasing of the second stage (x2) multiplier has to be optimized to achieve the maximum power of harmonic at 1 GHz. The power of that Harmonic into 50 Ohm was -10 dBm, which allowed to attain targeted + 7 dBm of output power by using just one stage linear amplifier.
frequency and reference frequency are below the noise floor of the instrument.

Results

The phase noise plot of the developed OCXO is shown in Fig. 4. The goals of the development were met at frequency offsets close to the carrier and on the noise floor. The midsection of the plot did not meet our objectives due to the limitations of the PLL circuit used. Over temperature performance was defined by the reference OCXO ± 10 ppb over -20 to 70 ºC range. The spectral purity of the output signal is shown on Fig. 5.

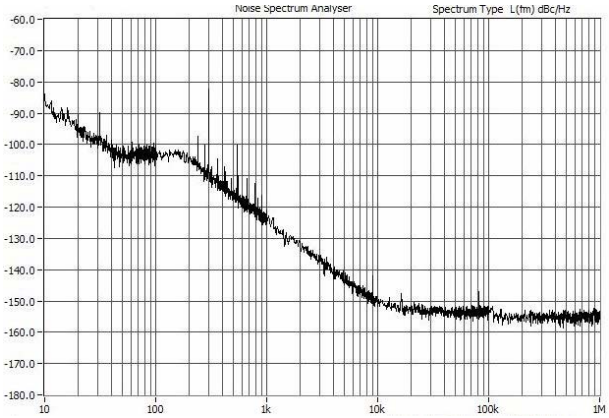

Fig.4. 1 GHz OCXO Phase Noise

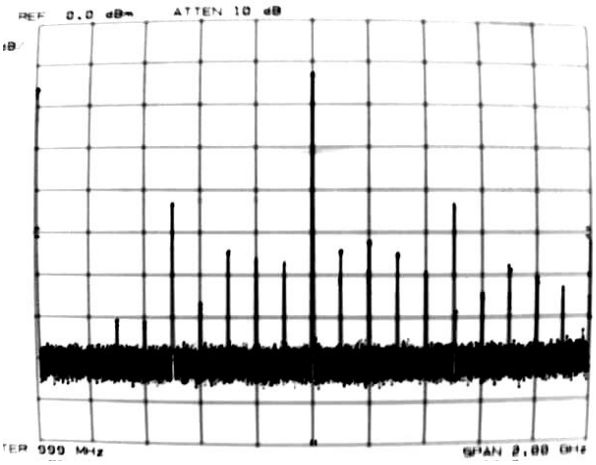

Fig. 5. Spectral purity of 1 GHz OCXO

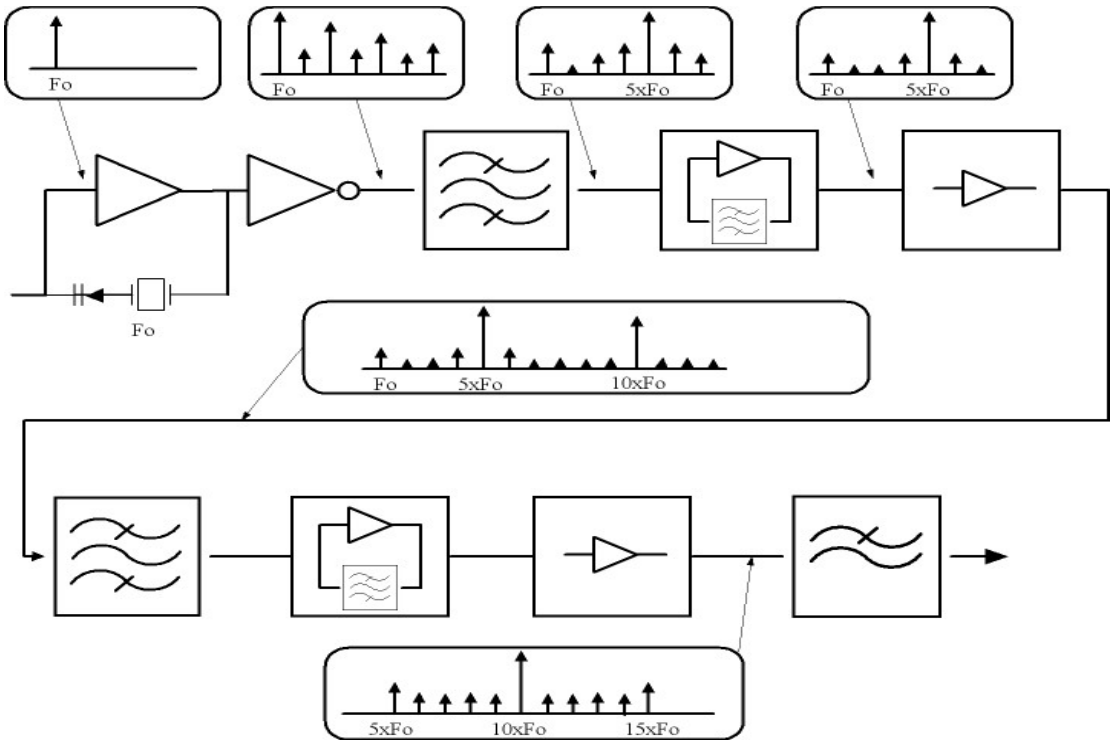

Fig.6. VCXO circuit block diagram with spectrum

Conclusion

1 GHz small form factor OCXO with exceptional phase noise and high output RF power was developed. The construction of the device is modular, which affords versatility. The resulted phase noise on the noise floor is below -150 dBc/Hz. Phase noise at 10 Hz offset from the carrier is close to -90 dBc/hz. Phase noise in 100 Hz to few KHz offset range is a subject for future improvement. Medium and long term stability is determined by the reference oscillator employed, which in this particular case provided temperature stability of ± 10 ppb in -20 to 70ºC temperature range and aging better

References:

1. R. Boroditsky, D.V. Bogomolov. Ultra low noise UHF TCXO. Proc. of 2005 IEEE Int. Freq. Contr. Symp.
2. R.Boroditsky, J. Gomez, S. San-Pedro. Ultra Low noise Stratum3 TCXO with High Output Power. Proc. Of 2006 IEEE Int. Freq. Contr. Symp.